IN THE CLAIMS:

Claim 1 has been amended herein. All of the pending claims 1 through 20 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently amended) A process for fabricating a contact structure for an integrated semiconductor circuit comprising:

providing a silicon region on at least a portion of a surface of a semiconductor wafer for making electrical contact thereto;

depositing a dielectric layer over the silicon region;

etching a contact opening through the dielectric layer for exposing a portion of the silicon region, the contact opening having a sidewall;

depositing a titanium metal layer within the contact opening to cover the portion of the silicon region exposed by the contact opening;

depositing an amorphous titanium carbonitride film having substantially no crystalline titanium therein, the amorphous titanium carbonitride film lining the sidewall of the contact opening and overlaying the titanium metal layer covering the portion of the silicon region exposed by the contact opening using a vapor deposition process when the semiconductor wafer is located in a chamber; and

filling at least a portion of the contact opening using a conductive material.

2. (Original) The process of claim 1, wherein depositing the amorphous titanium carbonitride film includes a chemical vapor deposition process.

3. (Original) The process of claim 2, wherein the chemical vapor deposition process includes:

evacuating a deposition chamber to a pressure of less than about 100 torr;

heating the semiconductor wafer to a temperature within a range of about 200° to about 600° C;

maintaining the temperature of the semiconductor wafer;

admitting an organometallic precursor compound into the deposition chamber, the organometallic precursor compound including a tetrakis-dialkylamido-titanium compound;

decomposing the organometallic precursor compound at or near the surface of the semiconductor wafer; and

depositing the amorphous titanium carbonitride film having substantially no crystalline titanium therein on at least a portion of the surface of the semiconductor wafer and within the contact opening.

4. (Original) The process of claim 3, wherein the organometallic precursor compound comprises tetrakis-dimethylamido-titanium.

5. (Original) The process of claim 1, wherein the conductive material comprises a metal selected from the group consisting of tungsten, aluminum, copper and nickel.

6. (Original) The process of claim 1, wherein the conductive material comprises doped polycrystalline silicon.

7. (Original) The process of claim 1, further comprising:

heating the semiconductor wafer; and

reacting at least a portion of the titanium metal layer covering the portion of the silicon region exposed by the contact opening with the silicon region to form a titanium silicide layer.

8. (Previously Presented) The process of claim 7, wherein reacting the at least a portion of the titanium metal layer with the silicon region occurs prior to depositing the amorphous titanium carbonitride film having substantially no crystalline titanium therein.

9. (Previously Presented) The process of claim 7, wherein reacting the at least a portion of the titanium metal layer with the silicon region occurs subsequent to depositing the amorphous titanium carbonitride film having substantially no crystalline titanium therein.

10. (Original) The process of claim 1, further comprising:

subjecting the amorphous titanium carbonitride film having substantially no crystalline titanium therein to rapid thermal processing in the presence of one or more gases selected from the group consisting of nitrogen, hydrogen and the noble gases.

11. (Previously Presented) An integrated circuit fabrication process for a contact structure comprising:

providing a silicon region on at least a portion of a surface of a semiconductor wafer for making electrical contact thereto;

depositing a dielectric layer over the silicon region;

etching a contact opening through the dielectric layer for exposing a portion of the silicon region, the contact opening having a sidewall;

depositing a titanium metal layer within the contact opening to cover the portion of the silicon region exposed by the contact opening;

depositing an amorphous titanium carbonitride film having substantially no crystalline titanium therein, the amorphous titanium carbonitride film lining the sidewall of the contact opening and overlaying the titanium metal layer covering the portion of the silicon region exposed by the contact opening using a vapor deposition process when the semiconductor wafer is located in a chamber; and

filling at least a portion of the contact opening using a conductive material.

12. (Original) The process of claim 11, wherein depositing the amorphous titanium carbonitride film includes a chemical vapor deposition process.

13. (Original) The process of claim 12, wherein the chemical vapor deposition process includes:

evacuating a deposition chamber to a pressure of less than about 100 torr;

heating the semiconductor wafer to a temperature within a range of about 200° to about 600° C;

maintaining the temperature of the semiconductor wafer;

admitting an organometallic precursor compound into the deposition chamber, the organometallic precursor compound including a tetrakis-dialkylamido-titanium compound;

decomposing the organometallic precursor compound at or near the surface of the semiconductor wafer; and

depositing the amorphous titanium carbonitride film having substantially no crystalline titanium therein on at least a portion of the surface of the semiconductor wafer and within the contact opening.

14. (Original) The process of claim 13, wherein the organometallic precursor compound comprises tetrakis-dimethylamido-titanium.

15. (Original) The process of claim 11, wherein the conductive material comprises a metal selected from the group consisting of tungsten, aluminum, copper and nickel.

16. (Original) The process of claim 11, wherein the conductive material comprises doped polycrystalline silicon.

17. (Original) The process of claim 11, further comprising:
heating the semiconductor wafer; and
reacting at least a portion of the titanium metal layer covering the portion of the silicon region exposed by the contact opening with the silicon region to form a titanium silicide layer.

18. (Previously Presented) The process of claim 17, wherein reacting the at least a portion of the titanium metal layer with the silicon region occurs prior to depositing the amorphous titanium carbonitride film having substantially no crystalline titanium therein.

19. (Previously Presented) The process of claim 17, wherein reacting the at least a portion of the titanium metal layer with the silicon region occurs subsequent to depositing the amorphous titanium carbonitride film having substantially no crystalline titanium therein.

20. (Original) The process of claim 11, further comprising:
subjecting the amorphous titanium carbonitride film having substantially no crystalline titanium therein to rapid thermal processing in the presence of one or more gases selected from the group consisting of nitrogen, hydrogen and the noble gases.